computing today No 2

December 78

Win a Triton

THE NEW MAGAZINE FOR SMALL SYSTEMS WITH BIG IDEAS ....

Simplified I/O
Microbiography
EPROM Programmer

Presented as a supplement to ETI.

computing today

No.2 December 1978

INTRODUCTION

We do not plan a regular editorial page in Computing Today for the simple matter that we'd soon run out of things to say — try looking at the editorial pages of other magazines for ample evidence of this.

This month, however, we'd like to take this opportunity of making the familiar plea of all new magazines — please let us know what you think of us we've had a couple of interesting comments on last month's issue but we would like to think we have slightly more than ten readers with something to say if you happen to have the odd article describing some aspect of personal computing we'd also be glad to hear from you.

Last month we omitted to credit the authors of a number of items to put the record straight Howard Birkett was responsible for the NASCOM 1 review, Phil Cornes for part 1 of the BASIC explained series and Don Scales for the item on the Triton's BASIC.

Errors noted in the Triton article are: 1) On page 31 of November's ETI the keyboard connection diagram should have shown the third output down on the right-hand side of the diagram as not strobe. 2) Strictly speaking the reset signal at the extender socket is not buffered and should have been marked as such.

Texas Talk

We've been hearing stories about Texas's entry to the hobby/education/business computer markets for some time. Like so many other Texas product launches before it, the stories around for months before the first sight of any hardware, lead to a sense of anti-climax at the official unveiling.

Hopes that the machines will not be waiting in the wings for too much longer, however, are strengthened by the fact that Texas's European Consumer Division have just appointed a personal computer manager.

The machine should be worth the wait for it is Texas's view that a late entry into a competitive field, such as home computing, means that the product must enter on a technological cusp. What will they offer us for our money. Views vary but most seem to suggest that the Texas machine will include some form of fast access, fast transfer, form of mass storage — (floppy?, Bubble??). We say the machine is expected soon — it must be — though we were disappointed when we heard the latest pronouncement on the reason for the delay — Texas did not want to get caught up on the Christmas novelty market and so had decided to launch next year.

The research machines 380Z system has been with us for some time now Z80 based, the system in its basic form consists of a by now familiar configuration — the 380Z itself with a standard domestic TV or video monitor to provide output and a cassette recorder for back up storage.

The recent addition of a mini-floppy system to the 380Z's hardware will greatly increase the scope of the system. The mini-floppy is offered with one or two drive's each with a 70K capacity BASF drives are used and the price includes Digital Research's CP/M disc operating system, rapidly becoming the industry standard for Microcomputers.

Research Machines will be able to offer several BASIC interpreters and compilers — FORTRAN and

News

COBOL will follow. In addition, purchase of the system from Research Machines will secure membership of the CP/M user's club with access at nominal cost, to the user's club library, already running at 14 volumes.

Singleboard Superboard

Due in this country before the end of this year, the Ohio Scientific Inc Superboard 2, is a machine to look out for. The system is built on a single board — even the keyboard is on the PCB — all that is required is a 5V 3A PSU.

Based on the 6502 MPU, PET, APPLE et al, with an 8K BASIC and up to 8K of static RAM, the Superboard 2 packs quite a processing punch.

The onboard keyboard is a 53 key design providing upper and lower case plus some user programmable functions. Also included is a Kansas City tape interface.

The output is to a video monitor and the display is a 24x24 format that provides graphics as well as alpha-numeric characters.

Available options include an expander board that features 24K of static RAM, a dual mini-floppy interface and a port adapter for printer and MODEM.

The machine — can you wait? — should be available here at a cost of £284.95 — what do you say about that Commodore?

People Like Petsoft

Petsoft have arranged a reciprocal deal with Personal Software Inc, a large American Microsoftware house, with the result that PETSOFT'S large range of software will now be distributed in the States and Canada and some of Personal Software's best titles will be available from PETSOFT.

The Microchess program (£14) is one example of Personal Software's work and at the low asking price, should be well received over here.

The PETSOFT catalogue is running at about 100 titles covering everything from games to business packages and software tools. An SAE to PETSOFT at the address below will secure their catalogue.

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PIAs Simplified

Ron Wilson explains the operation of a typical PIA (Peripheral Interface Adapter), clearing up the confusion often caused when a data sheet is consulted by a novice to the art of I/O. A 6800 based system is taken as an example for this article.

ON THE PIA THERE are 16 bi-directional lines that can individually be made to act as straightforward inputs or outputs. The 8 bit structure of the 6800 dictates that these lines are separated into an A group and a B group each of 8 bits. The internal register structure of the PIA is shown from the users viewpoint in Fig. 1. The A register group and the B register group each consist of a **Control Register, Data Direction Register,** and **Data Register**. It is to the data registers that the two sets of bi-directional data lines are connected. The 6800 system is organised so that the microprocessor treats the PIA registers as memory locations. The PIA can be addressed and will respond to instructions in the same way as memory.

The documentation that arrives with the ready-built microcomputer board obtained by the user will specify the PIA addresses for that system. A particular PIA might be located, for example, at addresses 8004 to 8007 inclusive. (The number system used is normally hexadecimal).

In this case the A side registers have been allocated 8004 and 8005 whereas the B side registers occupy locations 8006 and 8007. Each side has thus two addresses available to access three registers. How can three registers be accessed with only two addresses?

The address 8004 is given to two registers, the 'A' Data Direction Register and the 'A' Data Register. The required register is selected, from these two, by programming bit-two (b2) in the Control Register. The Control Register is at location 8005. When b2 is logic 0 the Data Direction Register is selected. Conversely when b2 is logic 1 the Data Register is selected. The user's aim is to configure output and input lines, so particular cases will now be illustrated.

The cases described have each been tested and work correctly. It will be shown how difficulties involved in obtaining input and output lines for direct use can be overcome. This will satisfy the initial demands of many microprocessor users. Where more complex strategies are required the interupt and handshake facilities of the PIA may need to be incorporated.

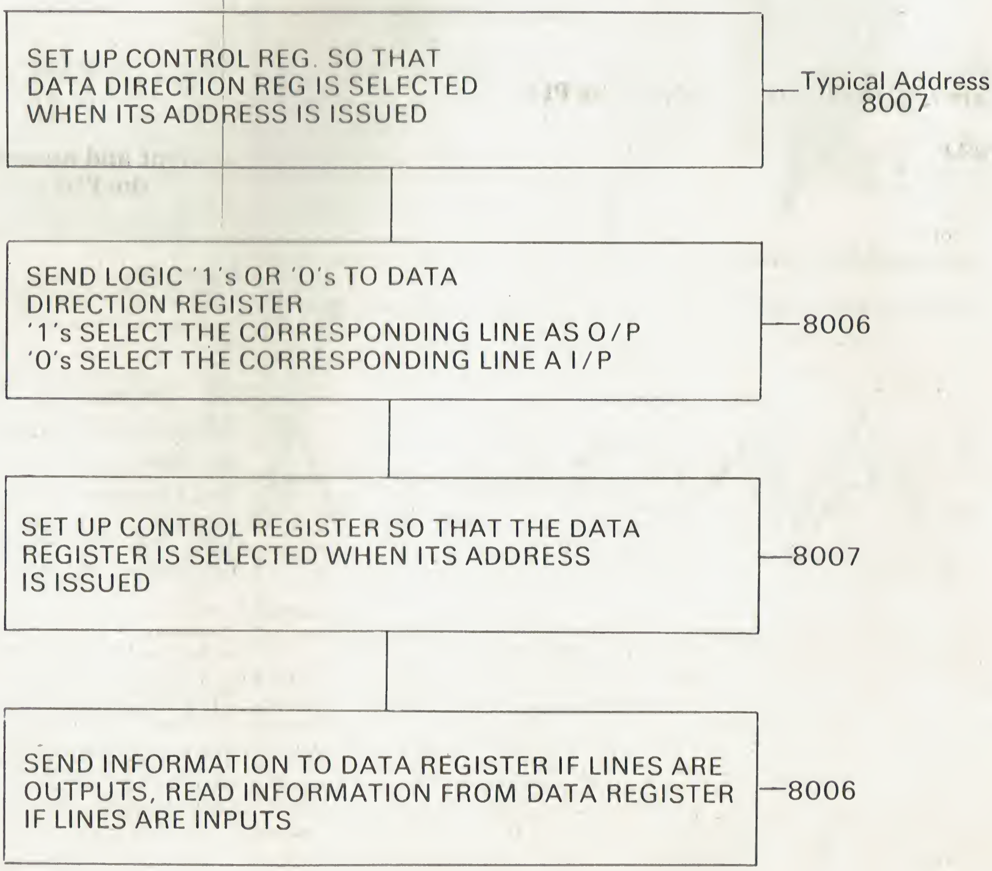

Fig. 2. The typical procedure adopted by a user when configuring a PIA to operate in any one of its available modes.

The Internal Registers of the PIA

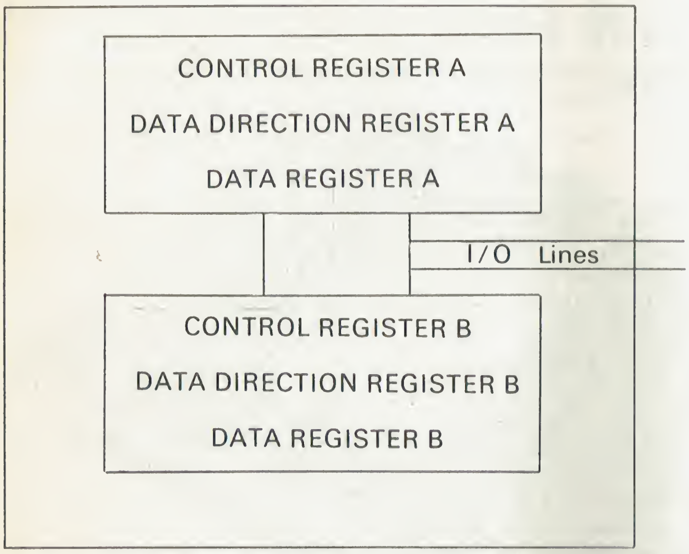

Fig. 1. The internal structure of a typical PIA. The Internal Register structure can be split into two distinct blocks each in turn consisting of a Control Register, Data Direction Register, and a Data Register. These Registers must be configured by the user to meet his requirements.

8 Output lines are needed on the B side of the PIA

POSSIBLE PREVIOUS PROGRAMMING

Code	mnemonic	Comments
86	LDA A	Load accumulator A with 0000 0000 (in binary)
00	00	
B7	STA A	Send accumulator contents to Control Register B.
80	80	As b2 = 0 the Data Direction Register B will be
07	07	accessed when address 8006 is next used.
86	LDA A	Load accumulator A with 1111 1111 (inbinary)
FF	FF	
B7	STA A	Send accumulator contents to 8006. This
80	80	establishes PIA B side as outputs. (A 1 configures
06	06	the corresponding line as an output.)
86	LDA A	Load accumulator A with 000 0100
04	04	
B7	STA A	Send accumulator contents to Control Register B.
80	80	As b2 = 1, next time 8006 is addressed the Data
07	07	Register is selected
86	LDA A	Load accumulator A with 0000 1111 as typical data
0F	0F	to be output
B7	STA A	Send this data to 8006. This now acts as output
80	80	information
06	06	

This program sets up the B side of the PIA as 8 output lines then shows how to send out data along these lines. Address 8007 locates the Control Register with 8006 shared between the Data Direction Register and the Data Register.

Any data now sent from the microprocessor 8006 will act as output information. The code is the assembled version, written in hexadecimal, of the instruction mnemonic.

The sequence involved in setting up the PIA for output and/or inputs can be generalised as shown in Fig. 2.

8 Input lines are required on the A side of the PIA

POSSIBLE PREVIOUS PROGRAMMING

Code	mnemonic	Comments
86	LDA A	
00	00	Control Register A is set so that
B7	STA A	when 8004 is addressed the Data
80	80	Direction Register is selected.
05	05	
86	LDA A	
00	00	The A side of the PIA is established
B7	STA A	by setting the Data Direction Register A
80	80	to 0000 0000
04	04	
86	LDA A	
04	04	Control Register A is set so that when
B7	STA A	8004 is next addressed the Data Register
80	80	is selected and the input data read
05	05	
B6	LDA A	Load into accumulator A the input data
80	80	from 8004
04	04	

Address 8005 locates Control Register A with 8004 shared between the Data Direction Register and the Data Register. The generalised diagram of figure 2 has been used to derive this program.

The 8 lines connected to the A side act as inputs to the microprocessor system. The data on these lines can be loaded into, say, accumulator A for further processing. The use of the LDA A instruction at the end of the previous program makes use of tha extended addressing mode. The location 8004 is treated as a memory location and the instruction efficiently transfers the data present on the input lines to the accumulator.

A combination of input and output lines on side A of the PIA

code	mnemonics	Comments
86	LDA A	
00	00	Control Register A is set so that
B7	STA A	when 8004 is addressed the Data Direction
80	80	Register is selected
05	05	
86	LDA A	The A accumulator is loaded with
E0	E0	111 00000 (in binary). This is sent to
B7	STA A	Data Direction Register A to establish
80	80	b7, b6, b5 as outputs and b4, b3, b2, b1, b0
04	04	as inputs.
96	LDA A	
04	04	Control Register A is set so that when
B7	STA A	8004 is next addressed the Data Register
80	80	is selected.
05	05	

It is a characteristic of the PIA that individual lines in an 8-bit group can be programmed to be inputs or outputs. Normally input lines are grouped together and output lines are grouped together. In the following case five input lines and three output lines are required on the A side of the PIA. The three output lines are arranged to be on lines, 5, 6 and 7 with the input lines 0 to 4. (The most significant bit position is line 7).

The input data can read into accumulator A by using LDAA in extended mode on location 8004. Data can be output from an accumulator by using STA instruction on location 8004. Only the 3 most significant bits will be effective as outputs from the accumulator data.

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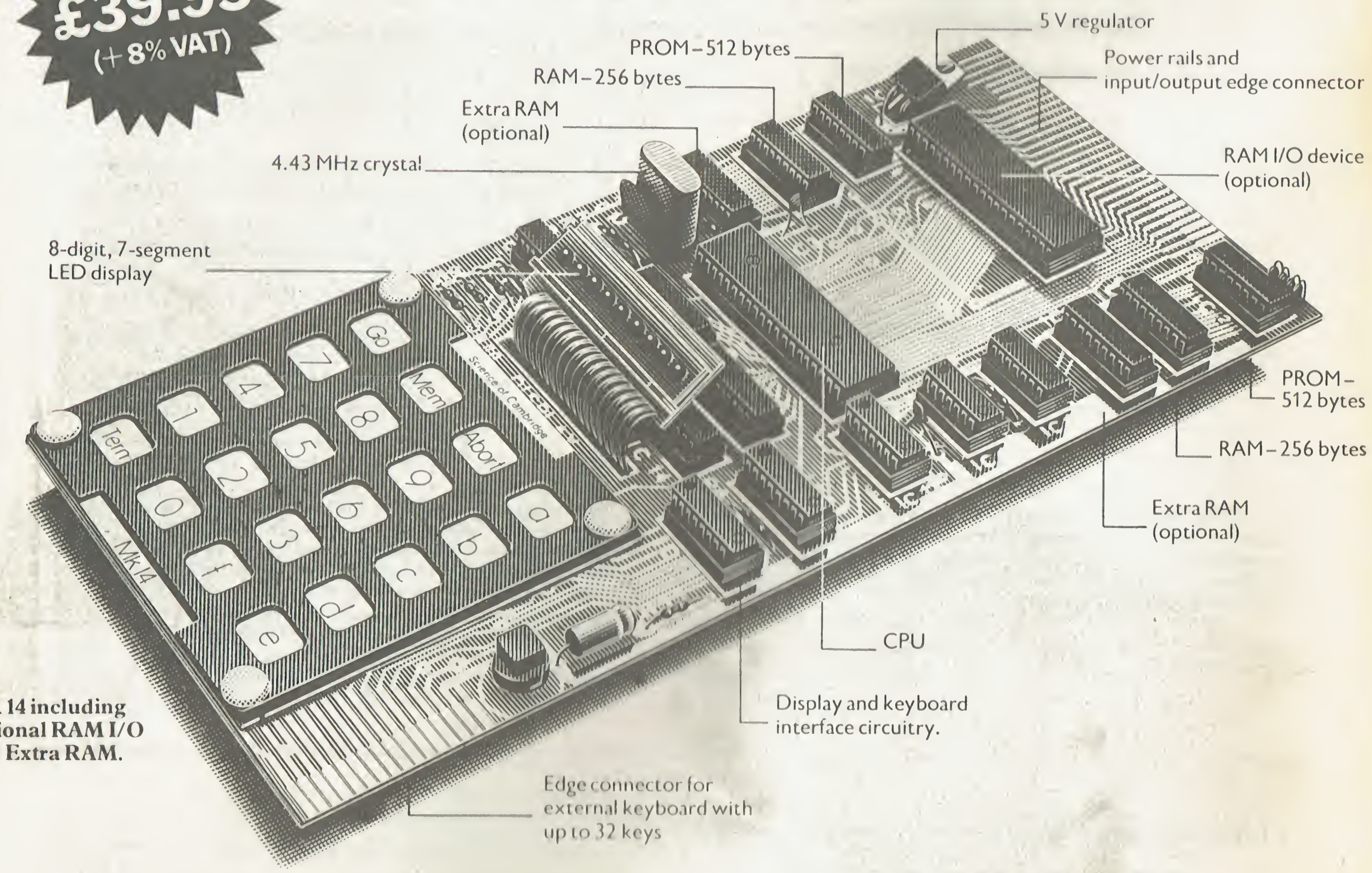

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SPECIFICATIONS

MK 14

* Hexadecimal keyboard
* 8-digit, 7-segment LED display
* 8 x 512 PROM, containing monitor program and interface instructions
* 256 bytes of RAM
* 4 MHz crystal
* 5 V regulator
* Single 8 V power supply
* Space available for extra 256-byte RAM and 16 port I/O

Edge connector access to all data lines and I/O ports

Optional Extras

* Extra RAM – 256 bytes
* RAM I/O device

Beginning BASIC

Part 2 of our series looks at some of the more common BASIC statements.

THERE ARE SEVERAL dialects of BASIC in service at present, depending upon which machine you are programing for, and so we will make a start by looking at those parts of the BASIC language which are more or less universal.

The first thing to do is to define a few terms which we will be using throughout the rest of the series.

VARIABLE

A variable is a character (or sometimes group of characters) to which a numerical value may be assigned. The most common variable names and those which are used by most machines are the 26 single letters of the alphabet (A to Z). Other examples of variable names will be pointed out as we come across them.

ARITHMETIC OPERATOR

There are five common arithmetic operators in BASIC.

'=' – to be replaced by the value of (read as 'equals') equality operator
'+' – addition operator
'–' – subtraction operator
'*' – multiplication operator
'/' – division operator

Some machines have a sixth arithmetic operator '↑' which means 'raised to the power of' (may also be written as '**').

COMPARISON OPERATORS

There are six common comparison operators.

'=' – equals
'<' – less than
'>' – greater than
'<=' – less than or equal to
'<>' – not equal to (can also be '≠')
'>=' – greater than or equal to

LOGICAL OPERATORS

There are two common logical operators.

'*' – logical AND (may be written as AND)
'+' – logical OR (may be written as OR)

Some machines also have a third logical operator – logical NOT (may be written as '~' or as 'NOT')

COMMAND

'Command' is the name given to keywords in BASIC which are used outside programs such as RUN, LIST, NEW etc. We will look at these in more detail later.

STATEMENT

The single instructions which go towards making up a program in BASIC are each called statements.

EXPRESSION

An expression is a collection of variables and/or numbers joined together by one or more arithmetic operators (so that 3*X+4, A—2 and A*(A+B)/(2—C) are all examples of expressions).

EQUATION

An equation is formed when an expression is assigned to a variable (so that Y=3*X+4, B=A—2 and Q=A*(A+B)/(2—C) are all examples of equations).

There is one other thing which should be discussed at this time. It can be described as follows—

If we let X take a value of 2 then what value do you think will be assigned to Y in the following equation.

Y=3+X*X

If you thought the answer was anything other than 7 or 10, then you want to brush up on your maths. If you thought the answer was 7 then you are probably wondering where 10 came from and vice-versa. It all depends on whether you used a calculator or a computer to work it out. If you used a calculator then you would have worked it out like this—

Y=(3+X)*X or Y=(3+2)*2

executing the operators as they occur and getting an answer of 10.

If, on the other hand, you used a computer, then you would have worked it out like this—

Y=3+(X*X) or Y=3+(2*2)

receiving an answer of 7. This may seem strange, but when computers do calculations they deal with the arithmetic operators in a certain order. First the computer scans the line left to right and performs all the multiplications and divisions as it encounters them; it then goes through again performing all the additions and subtractions that are left. The only way to alter the order of operations is to insert brackets where appropriate because the computer will work out the value of brackets before it does anything else and if there is more than one set of brackets one within another, it will work out the innermost brackets first.

So that, for example—

3+(2*(3+1*3))/(2+1)

has a value of 7 by the following reasoning.

The innermost brackets contain 3+1*3 which gives 6:3+(1*3): moving out to the outermost brackets we multiply this by 2 to give 12. This is one partial solution. We then move on to the last pair of brackets containing 2+1 and evaluate this as 3. That takes care of all the brackets and gives an expression which looks like this—

3+12/3

Division now comes before addition and this reduces to—

3+(12/3) or 3+4

then the addition is done to give a final answer of 7.

Try evaluating the following expression—

7+((7*8)/2)/(((12+8)*2)/20)

When you have done this, try taking out all the unnecessary brackets (parentheses) without re-arranging the order of the numbers (constants) and arithmetic operators so that the resulting expression gives the same result. The answers are given at the end of the article.

Certain facilities are required from any high level language, BASIC being no exception.

1. There must be a way of assigning values to any variables used in a program;
2. A method of outputting answers is also a must;
3. The language must have branching capabilities and in particular conditional branching must be provided;
4. Other facilities such as subroutines, string handling and some pre-defined functions are also useful and are usually provided.

LET

In BASIC the easiest way of defining a variable is to use a LET statement.

```
10 LET X=3
20 LET Y=X—2
30 LET T=T+1
```

There are several things that you should notice here. Firstly, every instruction is preceded by a line number.

The computer, in executing a program in BASIC, does so in sequential line number order, starting with the lowest numbered line and going through to the highest numbered line except where a branching instruction is encountered in which case the next line number to be executed forms part of the instruction.

Secondly, the '=' sign in these instructions does not mean 'equals' in the normal sense of the word, but means 'to be replaced by the value of'. So that line 20, when translated into English, means something like this—

LET whatever exists now in the memory locations representing the variable Y 'be replaced by the value of' whatever exists now in the memory locations representing the variable X, minus 2.

This may seem a bit of a tongue twister (it would normally be read as "LET Y equal X minus 2") and has only been presented in this form to make line 30 a little easier to understand.

LET T=T+1

What does it mean?

Well, briefly, if the memory space for the variable T had a value of 2 before the execution of line 30, it would have a value of 3 after its execution. Got it? If not, refer back to the tongue twister, substituting the variables and constants from line 30 into line 20 where appropriate and read it through a couple of times until you have mastered this concept, because it is very important. You should now be able to see (if you read Part 1) that where the following flow chart box appears—

ADD 1 to A

this could now be replaced by a box containing the following BASIC statement—

LET A=A+1

It is reasonable to point out at this time that on most machines which can run BASIC the LET statement is optional so—

10 LET A=A+1
and
10 A=A+1

are equally valid statements so that where, last month, we encountered the following—

To be continued ▶

A = 1

we were (apart from line numbers) already considering BASIC statements.

GOTO

The simplest form of branching instruction in BASIC is the GOTO statement, an example of its use is seen below—

```
10 LET Y=1
20 LET A(Y)=Y*Y
30 LET Y=Y+1
40 GOTO 20
```

The format of the GOTO statement is quite straightforward. The keyword GOTO is followed by the number of the line to which you wish control of the program to be transferred. Therefore, this program segment would be executed in the following order—

10 20 30 40 20 30 40 20 etc

As well as the GOTO statement, a new type of variable has been introduced in this program segment; the single subscript variable (can be known as a one dimensional array) represented here by the variable name (A(Y). In Tiny BASIC as well as having single letters to represent variables (A, B, K, Y etc) you can also use variables of the following format—

A(1), A(2), A(10), A(50) etc

where A(1) is as different from A(2) as X is from Y (The ETI Triton uses the @ symbol for its one single subscript variable, the TRS-80 Level I uses A).

Can we think of a use for these new variables? Well, if we think back to last month's card shuffling routines, we came across the following—

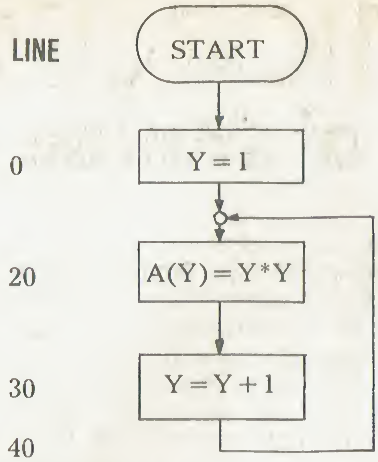
Put Random Number
R In Storage
Location A

where A took values from 1 to 52.

If we say that A(1) is storage location 1 and A(2) is storage location 2 or, in more general terms, A(A) is storage location A, then we have a representation for what was last month a set of 52 storage locations. So it is now obvious that the above flow chart box could be replaced by the following—

A(A) = R

Right! Let's go back to the program segment illustrating the GOTO statement.



This is its flow chart. We can see flow chart boxes representing lines 10, 20 and 30, but there is no box to represent the GOTO statement. It is merely represented by the box interconnection line which branches back to the connector between lines 10 and 20. While we are still on the subject, let's see what this program segment is actually doing (mentally executing a program without the aid of a computer is called DRY RUNNING a program).

Line 10 is the first line to be executed and all it is doing is assigning an initial value to the variable Y (in this case the value is 1). Now comes the line that might cause a bit of a problem.

20 LET A(Y)=Y*Y

If we think about the current value of the variable Y and substitute this value in the appropriate places, then what we end up with should make a lot more sense.

20 LET A(1)=1*1

All this says is "write 1(1*1) into the memory space representing the variable A(1).

Now we pass on to line 30, which we have met previously, and this line adds 1 to the memory locations representing the variable Y; so Y now has the value 2.

Line 40 is the GOTO statement which tells us that the next line to be executed is line 20 again, and so we go back and re-write.

20 LET A(Y)=Y*Y

as

20 LET A(2)=2*2

using the new value of Y so that we write 4(2*2) into the memory space representing the variable A(2). This process is now repeated for variables A(3) A(4) A(5) and so on. Unfortunately, we have included no method of stopping the program or of branching out of this loop as we have not yet covered such things, but bear with us and all will be revealed.

You may have noticed from the explanation so far given that this program segment is calculating the points for a graph of y=x and if we could look into the memory spaces representing the values of the variable A(Y) we would see the following—

A(1) . . . 1
A(2) . . . 4
A(3) . . . 9

One of the unfortunate points about this program is that it is an infinite loop (ie it will go on for ever with increasing values of Y) so we will now go on to look at a method of controlling the number of times we go round the loop.

TO BE CONTINUED

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MICROBIOGRAPHY

THE 8080

This month we begin a series of in-depth interviews with various CPU celebrities — starting with the device used in the TRITON.

THE INTEL 8080 has become an industry standard. For those of you with mainframe computing experience, it is the FORTRAN of processors — vast amounts of software are available for it and many people have experience of it.

It was for this reason that it was used in the ETI TRITON. Not only does it have its own software following, it will also run programs written for the earlier 8008 and the much more advanced Z-80 will (with a little help, no doubt) run 8080 programs, although writing for the Z-80 is more demanding.

What we hope to provide in this series of articles is enough information on a number of processors to enable the reader to decide which is best for a particular application.

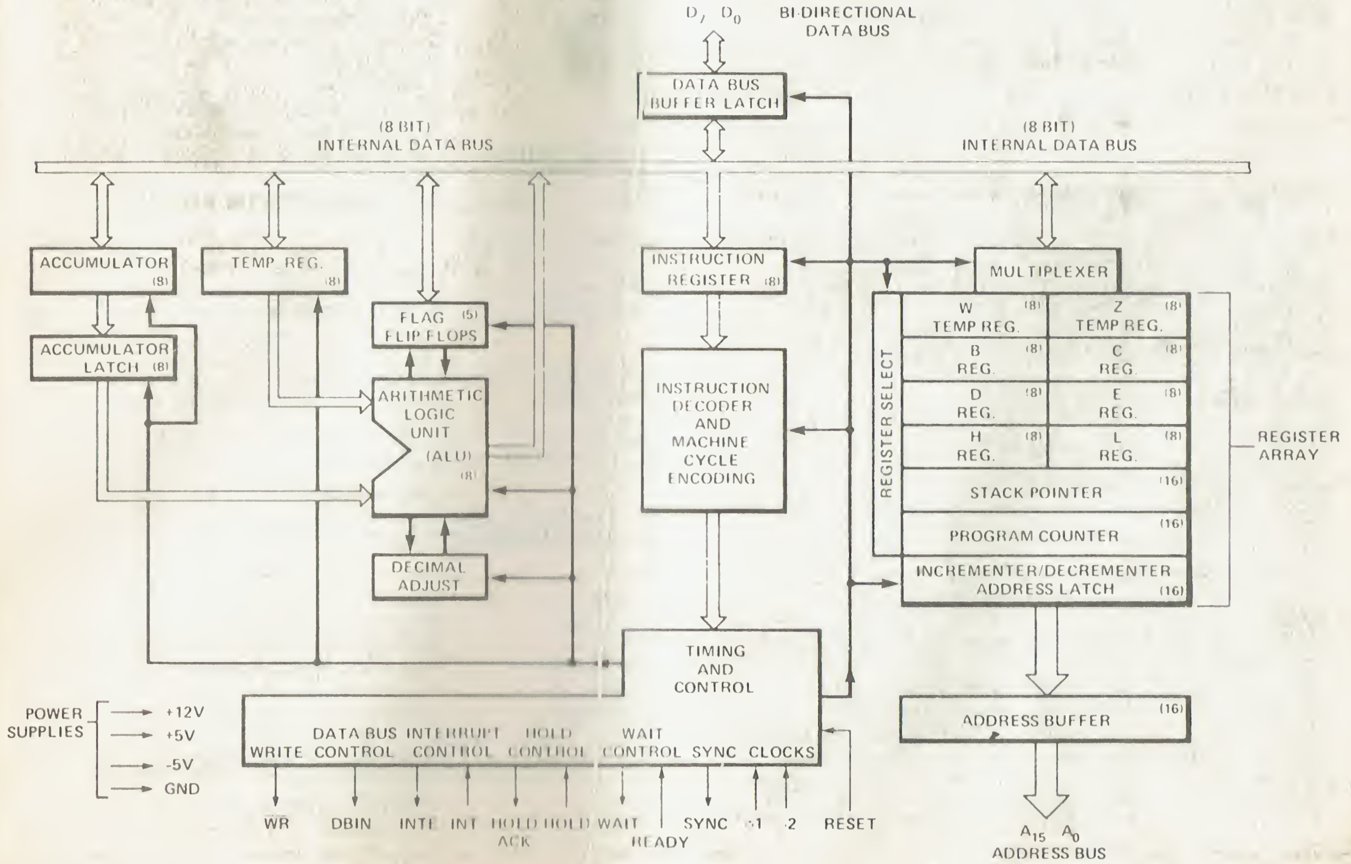
Registers

Not all of the registers shown on Fig. 1 are available to the programmer. The ones which are available are:

The accumulator;
registers B, C, D, E, H and L;
the stack pointer
and the program counter.

The accumulator

This is the scratch-pad of the CPU. Most instructions allow you to prod the accumulator in some way. The state of the contents of the accumulator affects the flags (see below).



Registers B, C, D, E, H and L

The CPU allows you to move data from register to register in this set but if you want to do anything clever to the data you have to put it into the accumulator.

Register pairs B&C, D&E, H&L and the stack pointer

Some of the instructions allow you to treat some pairs of registers as one 16-bit register (each individual register holds 8 bits). The allowable pairs are shown above. Most of these instructions can also be used on the stack pointer, which holds 16 bits.

Register pair H&L

Instructions which refer to a particular byte of memory usually do so by means of the H&L registers. The memory location is held in these registers (most significant 8 bits in the H register).

Program counter

This points to the position in the program which the CPU is at. By changing this (via jump instructions), the CPU can be made to jump to a different part of the program.

Stack pointer

One of the nice things about the 8080 is its ability to keep a stack in external memory automatically.

What is a stack, you ask?

A stack is like a stack of magazines. When you put data 'onto' the stack, the CPU will add 1 to the stack pointer and then put the data into the memory location which the stack pointer is 'pointing' at (i.e. the top of the pile). When you take data off the top of the stack, the CPU will copy it from the stack pointer location and then subtract 1 from the stack pointer.

This is very useful for interrupts, during which the CPU is asked to stop what it is doing and go and do something else. When this happens the CPU can save all the register contents by putting them onto the

THE 8080 INSTRUCTION SET

r stands for register eg A register
rp stands for register pair, eg b and C registers
'data' means the contents of the second or second and third bytes of the instruction
M stands for memory whose address is in the H and L registers

DATA TRANSFER GROUP

MOV r1, r2	Move register to register
MOV M, r	Move register to memory
MOV r,M	Move memory to register
MVI r, data	Move immediate (to register)
MVI M, data	Move immediate (to memory)
LXI rp, data 16	Load immediate (to register pair or to stack pointer)
STA addr	Store direct (accumulator to memory)
LDA addr	Load direct (memory to accumulator)
XCHG	Exchange H&L with D&E registers
STAX rp	Store accumulator indirect (with address in registers B&C or D&E)
LDAX rp	Load accumulator indirect (with address in registers B&C or D&E)
SHLD addr	Store H&L direct
LHLD addr	Load H&L direct

ARITHMETIC GROUP

INR r	Increment register
DCR r	Decrement register
INR M	Increment memory
DCR M	Decrement memory
ADD r	Add register to A
ADC r	Add register to A with carry
SUB r	Subtract register from A
SBB r	Subtract register from A with borrow
ADD M	Add memory to A
ADC M	Add memory to A with carry
SUB M	Subtract memory from A
SBB M	Subtract memory from A with borrow
ADI data	Add immediate to A
ACI data	Add immediate to A with carry
SUI data	Subtract immediate from A
SBI data	Subtract immediate from A with borrow
INX rp	Increment register pair (or stack pointer)
DCX rp	Decrement register pair (or stack pointer)
DAA	Decimal adjust A (gives two BCD digits)
DAD rp	Add B&C, D&E or H&L to H&L

LOGIC GROUP

ANA r	AND register with A
XRA r	EXCLUSIVE-OR register with A
ORA r	OR register with A
CMP r	Compare register with A
ANA M	AND memory with A
XRA M	EXCLUSIVE OR memory with A
ORA M	OR memory with A
CMP M	Compare memory with A
ANI data	AND immediate with A
XRI data	EXCLUSIVE-OR immediate with A
ORI data	OR immediate with A
CPI data	Compare immediate with A
RLC	Rotate A left
RRC	Rotate A right
RAL	Rotate A left through carry
RAR	Rotate A right through carry
CMA	Complement A
STC	Set carry
CMC	Complement carry

BRANCH GROUP

JMP addr	Jump unconditional
Jcond addr	Jump on condition specified (carry, no carry, zero, no zero, positive, minus, even or odd parity)
CALL addr	Call unconditional
Ccond addr	Call on condition specified (see above)
RET	Return
Rcond	Return on condition specified (see above)
RST	Restart
PCHL	H&L to program counter

STACK, I/O AND MACHINE CONTROL GROUP

HLT	Halt
IN port	Input (from port to A)
OUT port	Output (from A to port)
PUSH rp	Push register pair on stack (in memory)
PUSH PSW	Push A and flags on stack
POP rp	Pop register pair off stack
POP PSW	Pop A and flags off stack
XTHL	Exchange top of stack with H&L
SPHL	Move H&L to stack pointer
EI	Enable interrupts
DI	Disable interrupts
NOP	No op

THE 8080

stack. When the interrupt is over it can then read them back off the stack and go back to what it was doing.

This facility is also useful for subroutine calls.

Flags

A flag in this context is nothing to do with patriotism. It is one bit of a register which signals a particular condition.

There are five flags in the 8080's ALU: zero, parity, carry, auxiliary carry and sign.

All of them reflect the state of the data in the accumulator. They are accessed by means of the conditional jump class of instruction.

The interrupt enable flag (see Fig. 2) can also be set or reset by machine code instruction.

Instruction Set

Table 1 shows the 8080 instructions set.

The POP and PUSH instructions take data from and put data onto the stack, respectively.

The rotate class of instructions make the accumulator act like a shift register.

Increment and decrement add or subtract 1 from the relevent registers, respectively.

The NOP instruction is useful where there may be some changes in the program — to save shifting the rest of it to get more room.

Addressing Modes

The different ways in which the data following the machine code instruction byte can yield data are called 'addressing modes'. The ones which the 8080 uses are:

Immediate mode: Bytes 2 and/or 3 of the instruction contain the 8 or 16 bits of data to be used.

Direct addressing: Bytes 2 and 3 contain the address of the data in memory.

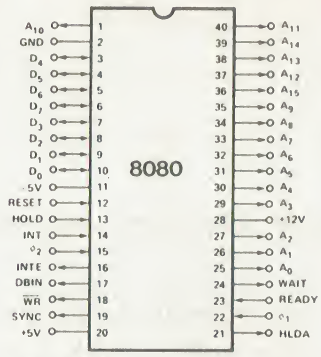
Register addressing: The instruction specifies which register the data is in.

Register indirect addressing: The instruction specifies a register pair (giving 16 bits) which is the address of the data in memory.

These modes are implicit in the description of the instruction set in Table 1 but the list shown above gives a useful overview.

Summary

The 8080 is a good general purpose CPU with adequate arithmetic operations. The instruction set is easy to follow and easy to use. The stack facility is nice, slightly marred by the lack of any single-byte stack instructions.



Pin Configuration

A0-A15: Address bus. Provides the address of a required memory location or I/O device number. Least significant bit = A0.

D0-D7: Tri-state bidirectional data bus. Least significant bit = D0.

SYNC: Indicates the beginning of each machine cycle.

DBIN: Indicates that the data bus is ready for data input.

READY: Tells the CPU that valid data is on the data bus, ready for input. If requiring data, the CPU will enter a 'wait' state until READY goes high.

WAIT: Active when CPU is in 'wait' state.

WR: Shows that the data bus carries valid output.

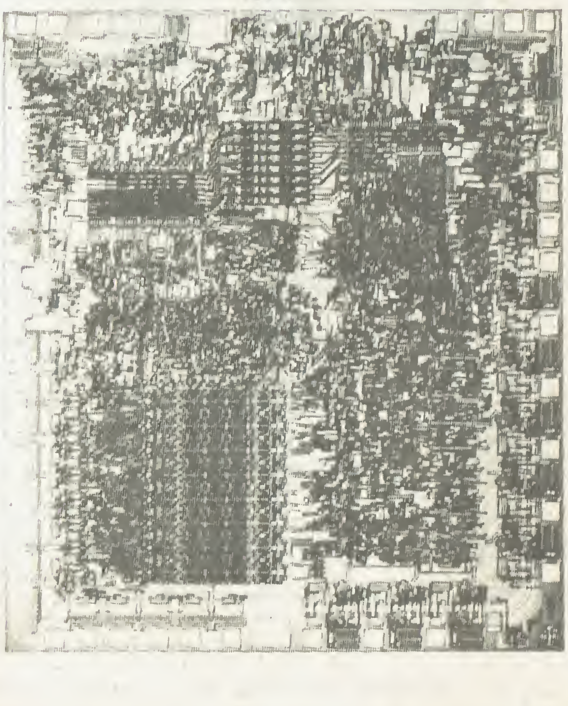
HOLD: Request to CPU to stop what it is doing and make the address and data busses high impedance.

HOLDA: High when CPU acknowledges the HOLD request and goes into a HOLD state.

INTE: INTE high means that the CPU will accept maskable interrupts. The state of INTE can be changed by the relevant machine code instruction.

INT: Interrupt request. Asks the CPU to jump to the relevant interrupt address.

RESET: Clears the program counter, INTE and HLDA.



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Solve the clues shown and enter them on the form below as though it were a cross-word but you will be entering numbers. In some cases leading zeros must be supplied.

Some of the clues are tough — but they are not tricks and those which you cannot answer from your head will be available in common reference books, from past issues of *ETI*, in particular the November issue featuring the TRITON. Note: Any arithmetic must be performed with TRITON's TINY BASIC's restrictions in mind.

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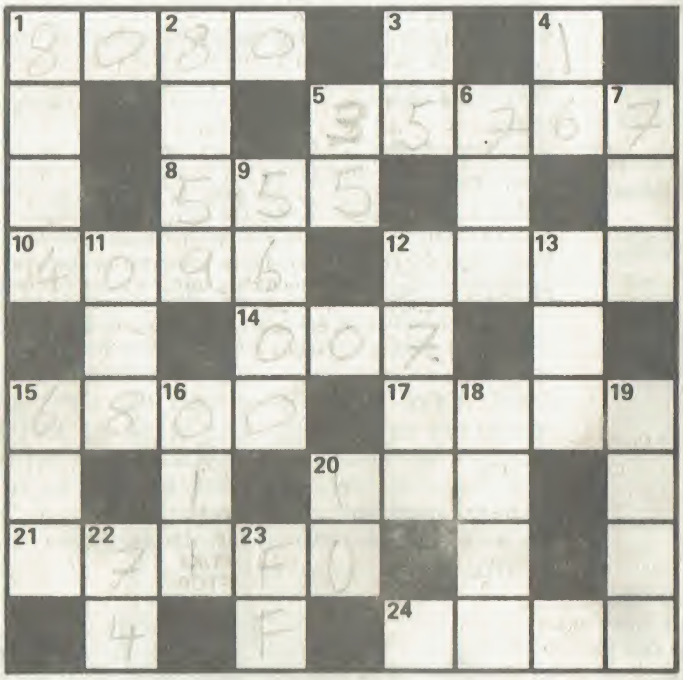


ACROSS

1. TRITON'S inteligent MPU
5. BASIC's largest number
8. Tick–tock UART's clock
10. 4K
12. 100*11+27+5/6
14. Secret agent
15. Motorola's best known MPU
17. Controlling influence for TRITON
20. Bit of a reverse (see16)
21. Needle in a STAC
24. Remember this IC

DOWN

1. Tick–tock TRITON's clock
2. Intel's programable interrupt controller
3. To to the fife.
4. No. of add. lines
5. Put a hex on 065 (Octal)
6. Operate on this amp.
7. The first is there, repeat for the rest
9. Green blue red (resistively speaking)
11. We've just ate here
12. Give us a ring
13. 24 across with nothing removed
15. 41/2+100*6–5
16. Backward 6 (in binary)
17. In control of TRITON
18. S.F. classic
19. Any port in a storm
20. Hecks its 4 down
22. Logic series
23. 8 bit MPU's max. address

Name ....

Address ....

....

CLOSING DATE DECEMBER 31st 1978

EPROM Programmer

Program your own 2708 EPROMS by connecting this project up to your systems serial port.

MOST HOBBYISTS now use EPROMs (Eraseable PROMs) of the 2708 type for the various firmware in their systems. 2708s are not now as expensive as they used to be, and have the advantage of allowing you to correct those inevitable bugs in your own programs or reuse the EPROM for some completely different program.

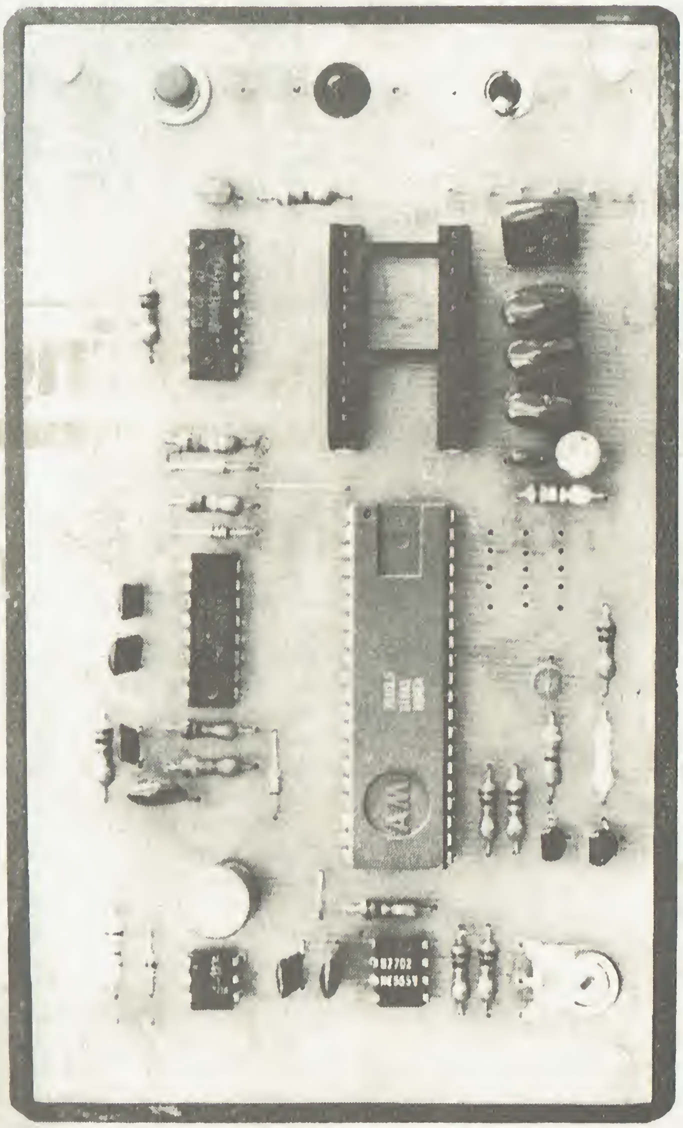
That's all very well, I hear you say, but I don't have a way of programing 2708s. Plus, commercial EPROM programmers are too expensive for me to justify since I only program one EPROM a month. Thanks to reader N. D. Hammond (and of course ETI) your troubles are over. Here is an inexpensive, nay, cheap, 2708 programmer suitable for individuals or impecunious clubs.

The programmer is, in fact, slightly different from the original design submitted to us by Mr Hammond; we have replaced some TTL in his design with CMOS and added a data time-out synchronisation facility, on which more later.

Design Features

The objectives of the original design were simplicity of construction and operation, and low cost. Another requirement which must be met is simplicity and versatility of interfacing — one of our bigger headaches is the fact that everyone's system seems to be different.

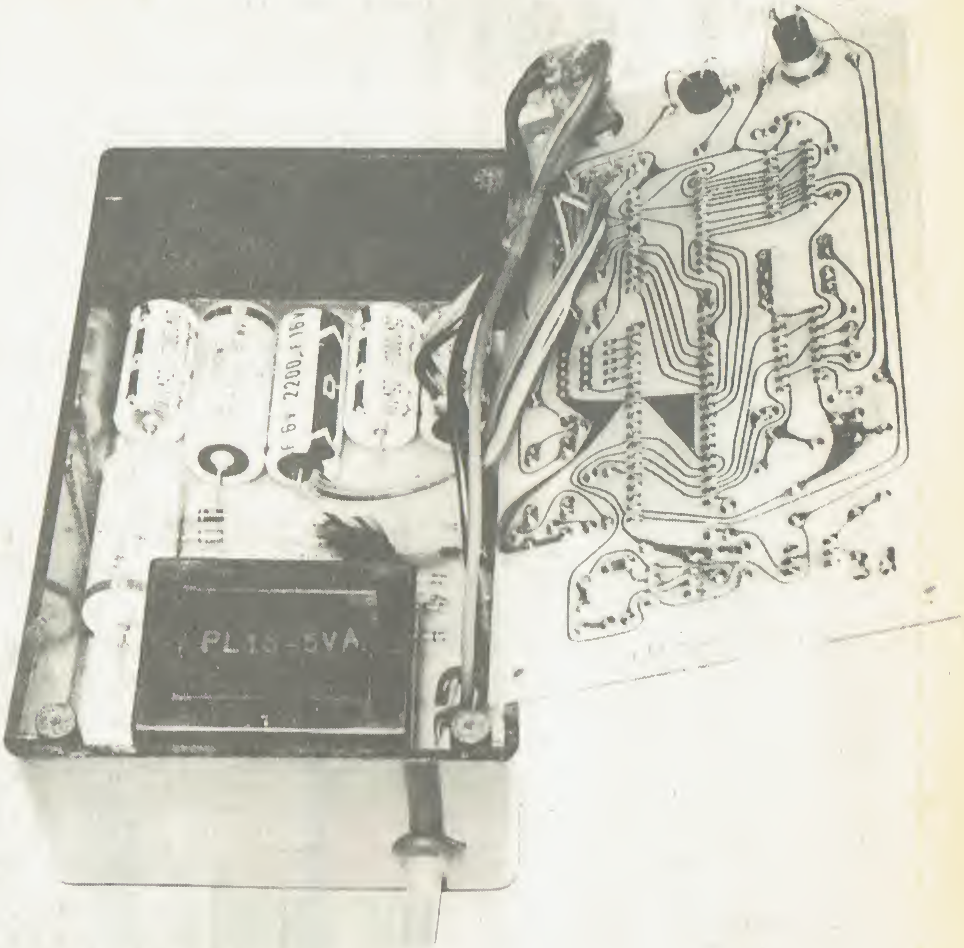
This project meets these objectives very well. The interface to the user's computer is *serial*, i.e. through a 20 mA current loop. As a bonus, the UART and a couple of one-shots provide all the necessary timing signals, so the component count is low and cost is low.



A useful by-product of our switch to a completely CMOS design was a spare gate, which we put to good use in providing a 'synchronisation' facility. The idea is that if a supply glitch or noise causes the UART to miss a byte of data, so that the 2708 addressing is out of step with the desired addressing, a ¼ second pause at the end of each cycle will reset the 4040 to zero. This means that only that cycle will be affected and subsequent cycles will be correct, increasing the programmer's tolerance to glitches.

There is one slight penalty that has to be paid — at 300 baud, it will take about 70 minutes to output all 1024 addresses 125 times. This is by no means brilliantly fast compared to the theoretical minimum programming time of 104 seconds but it is a lot better than the several days that would be required by a commercial firm.

Mr Hammond originally supplied software for the 8080, but our tests of the circuit were done on a MEK6800D2, for which we have written a routine, reproduced here. Our routine incorporates a time delay of approximately ¼ second at the end of each run through the 2708 addresses, in order to take advantage of the time-out synchronisation feature. Mr Hammond's 8080 program does not include this facility, but it is easy to add a time delay loop which decrements (say) the BC pair using the DCX instruction. We hope to give this program next month (so much to do, so little time, sigh!), but Mr Hammond's routine should work with no modification.



Adjustment

Before adjusting the oscillator frequency first fit the links which set the start-stop bit arrangement of UART.

Now with power connected adjust RV1 until IC2 is operating at 4800 Hz.

The 2708

At this point we digress to describe the 2708 and the steps involved in using and programming it.

The device is a static 8192 bit EPROM organised as 1024 x 8. It is packaged in a 24 pin DIP with a quartz window which allows the data stored in the memory to be erased by exposure to ultra-violet light.

Reading the device is quite straightforward. The appropriate address is applied at the ten address pins, the chip select pin is taken low and after the appropriate access time (120ns from CS or 450ns from address select) the data is available at the eight output pins.

Fortunately, and in contrast to its predecessors, the 2708 is also simple to program. The chip select pin is taken to the 'write enable' level of +12 V and the applied address is cycled from 000H to 3FFH with the appropriate data applied at each address. After the data and address lines have settled at each address, a 26 V pulse of 0.1 ms to 1 ms duration is applied at the programming pin. The entire cycle of 1024 addresses is repeated until each address has received a minimum of 100 ms program pulse time.

Erasure is the simplest operation of all. The window is uncovered and the chip placed an inch or so away from an ultra violet tube. After half an hour or so, the memory is fully erased (to all '1's) and is ready for re-programming.

Operation

A fully erased EPROM has every bit set to the '1' state. Programming sets selected bits to '0'. It follows that a 2708 can be reprogrammed without erasing if there are no cases where a bit must be changed from '0' to '1', otherwise the device must be erased by exposure to ultra violet light. Any 'germicidal' UV tube is suitable for erasing. The chip(s) should be placed about an inch or so from the tube and left for at least half an hour to ensure complete erasure.

To program the device, the pattern to be written should be available in RAM. The programmer

EPROM Programmer

Parts List

Main board

RESISTORS
(All ½W 5%)

R1,17	180R
R2,3,6,11, 13,15	10k
R4,5,12	1ko
R7	4M7
R8	180k
R9	100k
R10	470R
R14	33k
R16	47R

POTENTIOMETER

RV1	25k

CAPACITORS

C1	8n 2 polyester
C2-C4,6,7	10n polyester
C5	33n polyester
C8,9,11,12	100n polyester
C10	100u 25V electrolytic
C13	10u 35V electrolytic

SEMICONDUCTORS

IC1	4N33 Opto coupler
IC2	555
IC3	MM5303 UART
IC4	4049
IC5	4040
Q1	PN3638
Q2	BC548
Q3	BC558
Q4	BC548
D1-D4	1N914
LED1	

MISCELLANEOUS
PCB as pattern
24 pin IC socket
Push button
Plastic box 158x96x50mm

Parts List

RESISTORS
(All ½W 5%)

R1	1k
R2,3	120R
R4,5	47R
R6	470R
R7	100R

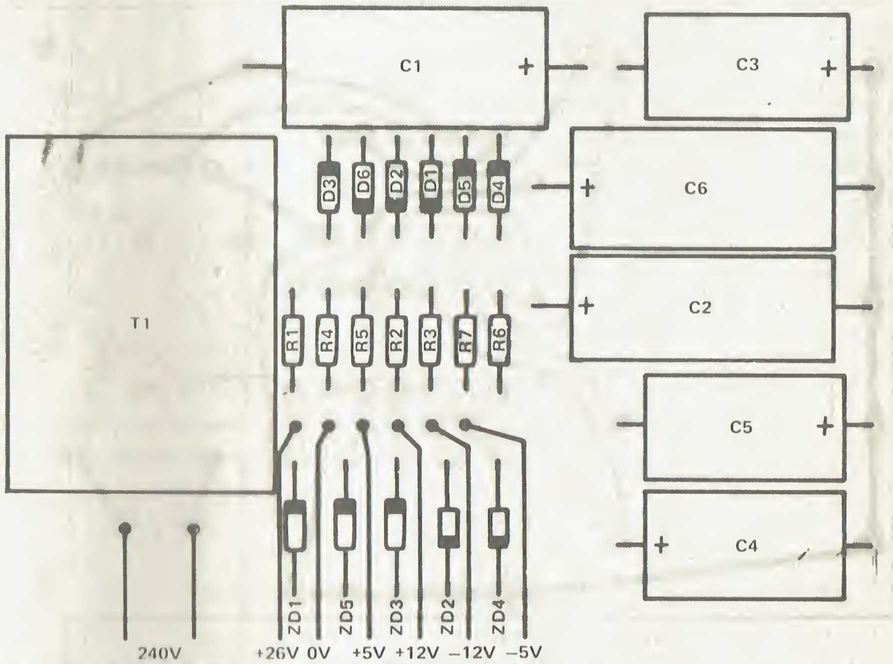
CAPACITORS

C1,6	470u 50V electrolytic
C2	2200u 16V electrolytic
C3-C5	1000u 25V electrolytic

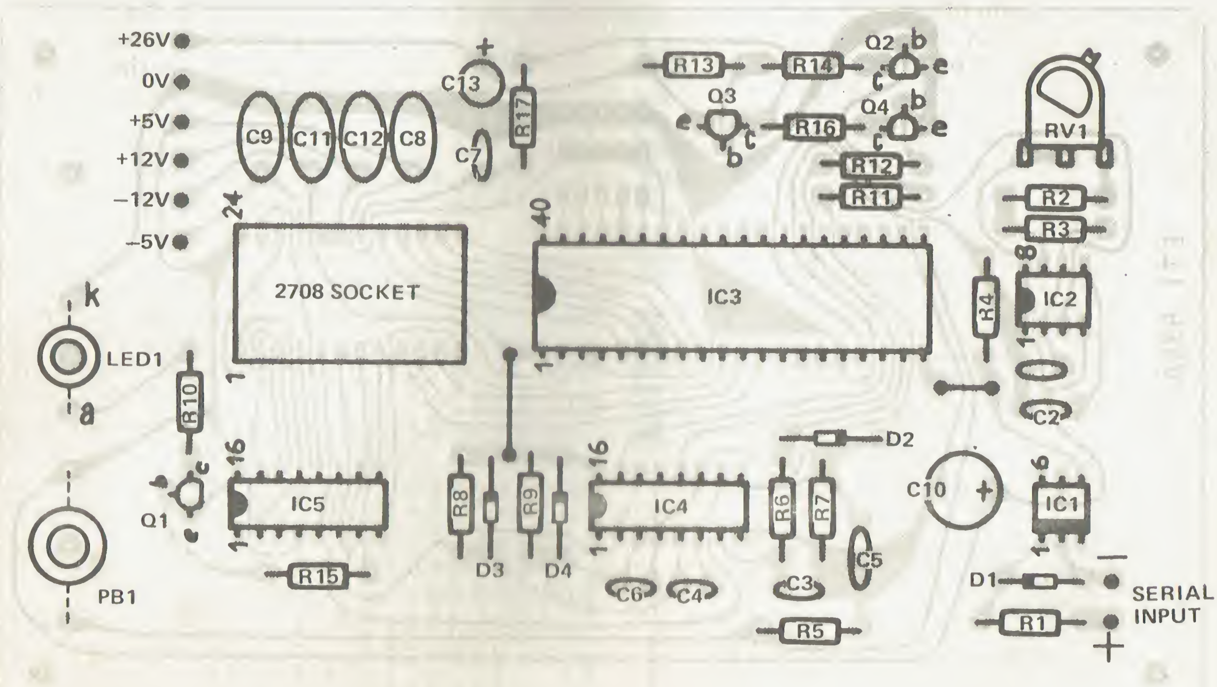
DIODES

D1-D6	1N4004
ZD1	27V 1W
ZD2	12V 400mW
ZD3	12V 1W
ZD4	5.1V 400mW
ZD5	5.1V 1W

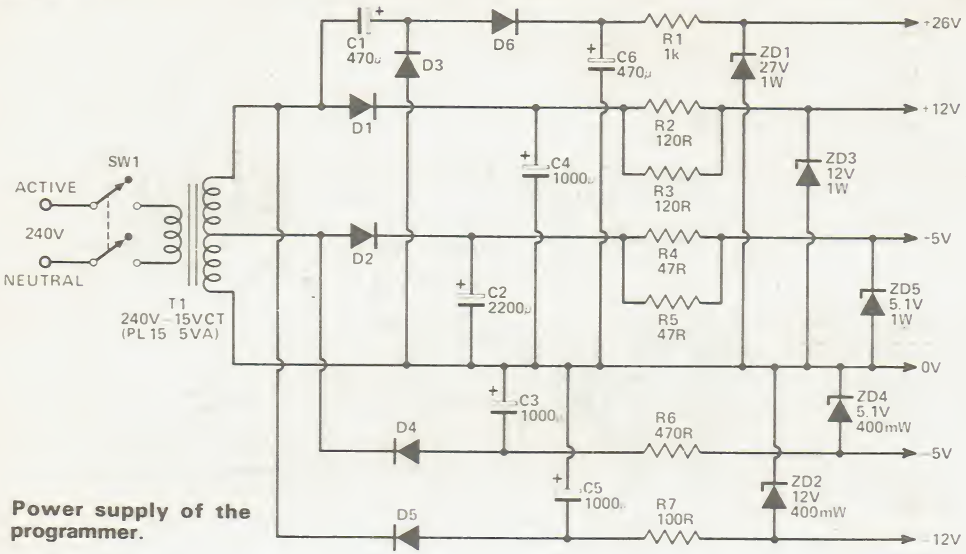
MISCELLANEOUS
PCB as pattern
Transformer PL15-5VA
Switch DPDT toggle
3 core flex & plug
Cable clamp



Overlay for the programmer main boards.



EPROM Programmer



Power supply of the programmer.

is connected to the microprocessor's serial port which is configured for the appropriate signal format selected for the programmer (see table 3). The programmer is then reset to initialize the UART and ensure that the address counter starts at address zero. All that remains is for the microprocessor to output the contents of the selected RAM page, byte by byte at the port. As the programming pulse width is approximately 1ms, the whole 1024 bytes should be output at least 100 times. In practice, this should be increased by 25% or so to allow for the effects of component tolerances.

Programmer Design

Use of the UART considerably simplifies the software requirements of the system which will drive the programmer, all that is necessary is a program which will output the required memory contents in order and repeat this for the required number of times.

How it Works

A fully erased EPROM has every bit set to the "1" state. Programming sets selected bits to "0". To program a 2708 the selected address and corresponding data has to be presented to the EPROM and a 26V pulse applied to the program input pin. To make life more difficult each location has to be selected and programmed in sequence. Also a total time the program input has to be high for each location is 100 ms but the pulse used cannot be less than 100µs or longer than 1 ms with about 1 ms recommended. This means that the IC has to be cycled through completely around 100 times for best results!

As we have a computer anyway (otherwise why the need for an EPROM!), we use it to provide the sequencing and timing needed.

The computer is programmed to copy data in its memory (1024 bytes) and sequentially transmit in serial form each byte 125 times. It also pauses for about ¼ second each 1024 bytes.

The serial information is transferred from the 20 mA loop into a 0-5V signal by the opto coupler, IC1, whose output is fed into the input of the UART IC3. This IC then converts this information into parallel form on pins 5-12 which is presented to the EPROM on its data lines. This IC needs a clock input at 16 times the Baud rate (4800Hz for 300 Baud) and IC2 is used for this.

The address lines for the EPROM are supplied by IC5 which is a 12 bit binary counter (we use only the first 10 bits) and this is reset to zero when no data is being received. On pin 19 of the UART we have an output which goes high when the serial data has been received and after this has been delayed by about 100 µs (R6/C3) the output of IC4/1 goes low. This triggers a 1 ms monostable (C4, R8, IC4/3) which drives the transistors Q2-Q4 to provide a 26V pulse to pin 18 of the 2708. At the end of this 1 ms pulse a second mono is triggered (C6, R9, IC4/4), the UART is reset (pin 19 goes low again) and the address counter IC5 is incremented. The output (pin 19) of IC3 also charges C5 via D2 when it goes high. This causes the output of IC4/2 to go low allowing IC5 to be toggled (pin 11 of IC5 is the reset line). Provided the output of IC3 goes high regularly corresponding to data being received at 300 Baud C5 does not have time to discharge and the reset line remains low. If there is a pause at the end of a complete cycle the reset line will go high and will correct any error which may have been caused by a possible glitch.

The power indicator LED is driven by one of the outputs of IC5 and is turned on and off quickly indicating data is being received.

TABLE 2 – INTERFACE PROGRAM FOR 8080/Z80

```
                ;***** INTERFACE PROGRAM FOR 2708 EPROM PROGRAMMER *****
                ;
                PAGESTART:  EQU  04H           ;HIGH ORDER BYTE OF RAM ADDRESS
                                               ;   TO BE LOADED IN EPROM ADDRESS
                                               ;   ZERO – LOW ORDER BYTE IS ZERO
                NEXTPAGE:   EQU  08H           ;HIGH ORDER BYTE OF PAGESTART + 1024
                CTRL:       EQU  0             ;ADDRESS OF I/O STATUS & CONTROL PORT
                DATA:       EQU  1             ;ADDRESS OF I/O DATA PORT

                ;INITIALIZATION – NOTE: SYSTEM DEPENDENT  THIS SEGMENT WRITTEN
                ;FOR AN INTEL 8251 SERIAL I/O PORT
                ;
0000: 3E 4E                 MVI  A, 4EH        ;MODE INSTRUCTION: SELECT 1 STOP,
0002: D3 00                 OUT  CTRL          ;   8 DATA AND NO PARITY FORMAT
0004: 3E 11                 MVI  A, 11H        ;COMMAND INSTRUCTION  RESET 8251
0006: D3 00                 OUT  CTRL          ;   AND SET TX ENABLE
                ;
                ;MAIN PROGRAM
                ;
0008: 06 7D                 MVI  B, 125        ;NO OF PROGRAMMER CYCLES TO B
000A: 26 04     NEWCYCLE:   MVI  H, PAGESTART  ;HIGH ORDER ADDRESS OF BYTE 1 TO H
000C: 2E 00                 MVI  L, 0          ;LOW ORDER ADDRESS TO L
000E:           NEXTBYTE:
000E: DB 00     TESTPOINT:  IN   CTRL          ;READ I/O PORT STATUS
0010: E6 01                 ANI  01H           ;MASK ALL EXCEPT READY BIT
0012: CA 0E 00              JZ   TESTPORT      ;LOOP UNTIL READY BIT SET
0015: 7E                    MOV  A, M          ;MOVE SELECTED BYTE TO ACC
0016: D3 01                 OUT  DATA          ;   AND SEND TO PROGRAMMER
0018: 23                    INX  H             ;SELECT NEXT BYTE TO BE SENT
0019: 7C                    MOV  A, H          ;TEST CONTENTS OF H TO SEE WHETHER
001A: FE 08                 CPI  NEXTPAGE      ;   LAST BYTE HAS BEEN SENT
001C: C2 0E 00              JNZ  NEXTBYTE      ; IF NOT, REPEAT LOOP
001F: 05                    DCR  B             ;ELSE DECREMENT CYCLE COUNTER
0020: C2 0A 00              JNZ  NEWCYCLE      ;IF NOT FINISHED START NEW CYCLE
0023: 76                    HLT                ;ELSE HALT
```

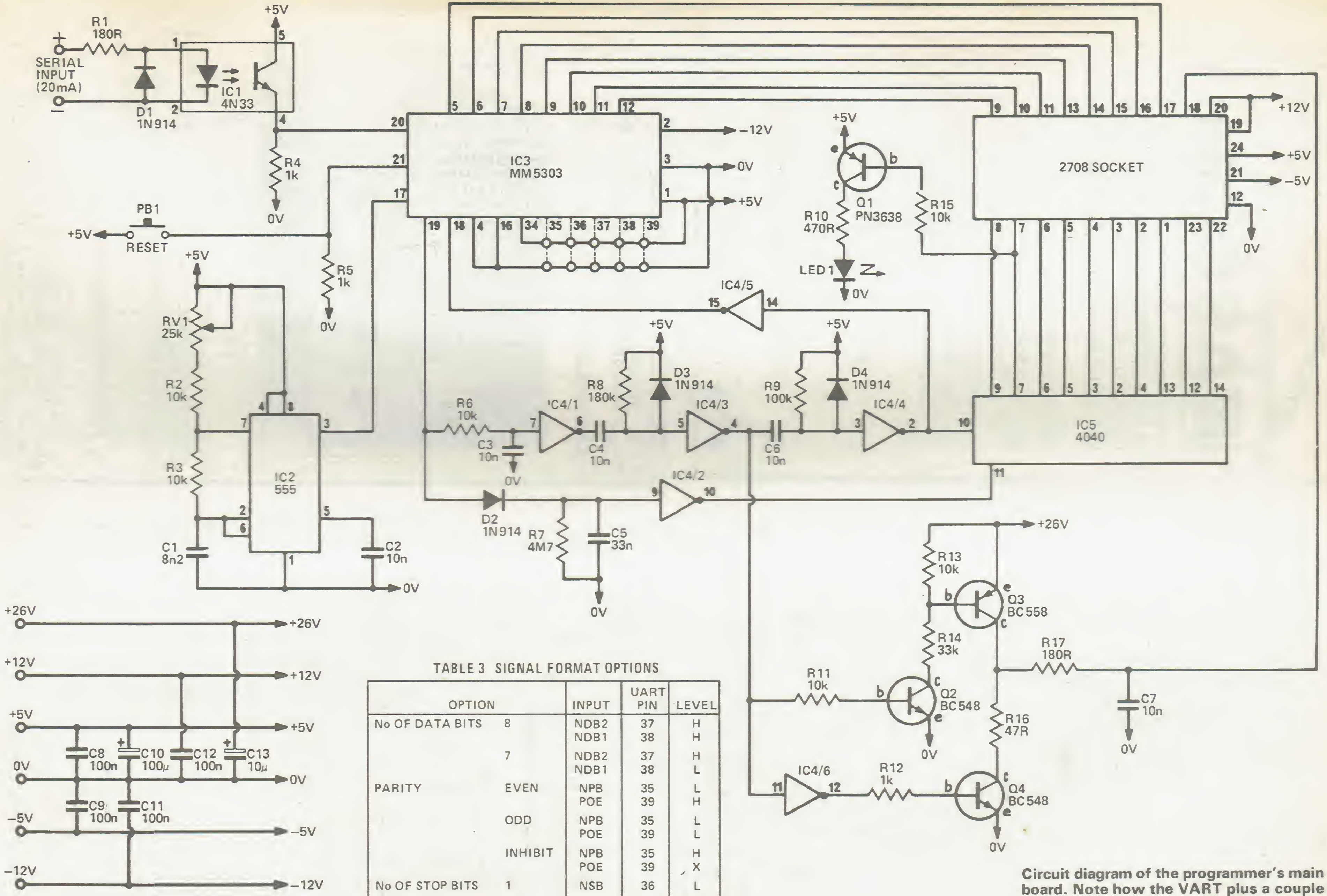


TABLE 3 SIGNAL FORMAT OPTIONS

OPTION		INPUT	UART PIN	LEVEL
No OF DATA BITS	8	NDB2	37	H
		NDB1	38	H
	7	NDB2	37	H
		NDB1	38	L
PARITY	EVEN	NPB	35	L
		POE	39	H
	ODD	NPB	35	L
		POE	39	L
	INHIBIT	NPB	35	H
		POE	39	X
No OF STOP BITS	1	NSB	36	L
	2	NSB	36	H

H=HIGH (+5V) L=LOW (0V) X=DON'T CARE

Circuit diagram of the programmer's main board. Note how the VART plus a couple of one-shots provide all the necessary timing signals.

Construction

We built our prototype into a plastic box with the power supply on one board in the box itself while the logic board was used in place of the lid.

These boards should be assembled according to the overlays provided. Normal handling procedures should be taken with the CMOS ICs and the UART. A good quality socket should be used for the EPROM as it will be used a lot. The pushbutton, LED and power switch are mounted on the logic board and connected from the rear.

With the power switch, due to the closeness of the capacitors on the lower board, the wires should be taken parallel to the PCB and the rear of the switch epoxied over to give protection. The connection between the power supply and logic board can be done with a piece of ribbon cable as the connections follow the same sequence.

We used PC pins for the data input points but a socket could be used if desired.

The PCB patterns for this project can be obtained by sending an SAE to Computing Today, 25-27 Oxford Street, London, W1R 1RF. Mark the envelope EPROM foils.

TABLE 1. 6800 EPROM DRIVER FOR D2

6800 EPROM PROGRAMMER DRIVER FOR D2

```
               OUTCH       EQU    E37A
               PAGESTART   EQU    04
               NEXTPAGE    EQU    08
               ACIAS       EQU    8008
               ; INITIALISATION OF ACIA
0000  86  55                          LDA  A   # %0101001
0002  B7  80   08                     STA  A
               ; MAIN PROGRAM
0005  C6  7D                          LDA  B     125
0007  CE  00   00   NEWCYCLE:  LDX  PAGESTART
000A  A6  00        NEXTBYTE:  LDA  A,    X
000C  BD  E3   7A                     JSR  OUTCH
000F  08                              INX
0010  8C  04   00                     CPX  NEXTPAGE
0013  26  F5                          BNE  NEXTBYTE
0015  36                              PSH  A
0016  37                              PSH  B
0017  86  FF                          LDA  A     $FF
0019  C6  FF                          LDA  B     $FF
001B  5A                   LOOP:      DEC  B
001C  26  FD                          BNE  LOOP
001E  4A                              DEC  A
001F  26  FA                          BNE  LOOP
0021  33                              PUL  B
0022  32                              PUL  A
0023  5A                              DEC  B
0024  26  E1                          BNE  NEWCYCLE
0026  3F                              SWI

For Test:
000A  86  XX        NEXTBYTE:  LDA  A      XX
outputs ASCII character XX
 or
000A  4C            NEXTBYTE:  INC  A
000B  01                       NOP
outputs incrementing characters.
```

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Softspot

The start of a regular software section in Computing Today this month. To start the ball rolling we present a game, designed to run on the TRITON, written by Don Scales. This section will not be restricted to BASIC programs however we want to publish machine code routines, even programming hints.

Send any software you have to Computing Today, 25-27 Oxford Street, London, W1R 1RF.

MISSILE (1K)

Missile is a game which utilizes the graphics and memory mapping features available to the TRITON.

The object of the game is to shoot down each enemy aircraft before it gets past your defences (across the screen). To do this you command three missile sites.

Unfortunately, your radar station has been knocked out and the aircraft can come in at any height between 1 and 16 miles high.

The missile stations are sited at 16, 32 and 48 miles from the coast (left edge of the screen). Both the aircraft at 8 miles high, station 1 must fire with a delay of 8 seconds.

There are 10 aircraft coming in and before each, you must set the missile fuses by specifying the time delay before ignition.

Good Luck.

```
10 N=0
20 FOR J=1 TO 10
30 @ (2)=976, @ (5)=992, @ (8)=1008
40 @ (3)=976, @ (6)=992, @ (9)=1008
50 PRINT 'MISSILE'
60 INPUT '1ST' @(1), '2ND' @(4), '3RD' @(7)
70 VDU 0, 12
80 FOR I=1 TO 150; NEXT I
90 Y=(RDN (16) — 1) *61, Z=1
100 FOR X=1 TO 64
110 VDU 2, 32
120 W=Y+X
130 VDU W, 62
140 Z=W
150 FOR I=1 TO 7 STEP 3
160 IF X <@ (I) GOTO 250
170 VDU @ (I+2), 32
180 IF @ (I+1) < 1 GOTO 250
190 VDU @ (I+1), 94
200 @ (I+2)= @ (I+1)
210 @ (I+1)= @ (I+1) —64
220 IF @ (I+2)=W GOTO 400
250 NEXT I
300 NEXT X
310 GOTO 500
400 VDU W, 42
410 N=N+1
500 NEXT J
510 PRINT 'HITS', N
```

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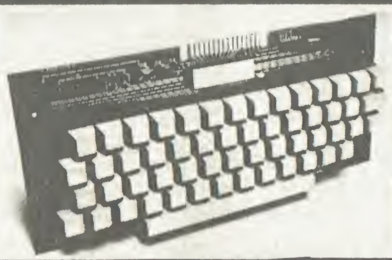

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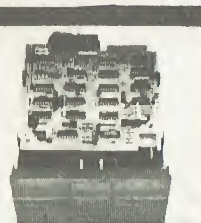

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